IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate;

a gate dielectric formed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a film formed adjacent to said semiconductor body wherein said film produces a stress in said semiconductor body.

2. The semiconductor device of claim 1 wherein said film produces a compressive stress in said semiconductor body.

3. The semiconductor device of claim 1 wherein said film produces a tinsel stress in said semiconductor body.

4. The semiconductor device of claim 1 wherein said film has tinsel stress.

5. The semiconductor device of claim 1 wherein said film has a compressive stress.

6. The semiconductor device of claim 5 wherein said compressive film comprises silicon nitride.

7. The semiconductor device of claim 1 wherein said semiconductor body is a single crystalline silicon film.

8. The semiconductor device of claim 1 wherein said semiconductor is selected from the group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

9. A tri-gate transistor comprising:

a single crystalline silicon body formed on insulating substrate, said silicon body having a top surface opposite a bottom surface and a first and second laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body and on said first and second laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric and on said top surface of said silicon body and adjacent to said gate dielectric on said first and second laterally opposite sidewalls of said silicon body;

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode; and

a stress induced film formed around said silicon body and said gate electrode, said film providing stress in the channel region of said device.

10. The method of claim 9 wherein said thin film has a compressive stress and places a tinsel stress in said channel region.

11. The semiconductor device of claim 10 wherein said thin film comprises a silicon nitride film.

12. The semiconductor device of claim 9 wherein said thin film has tinsel stress and incorporates a compressive stress into said channel region of said semiconductor body.

13. The tri-gate transistor of claim 10 wherein said semiconductor body channel region is doped to a p type conductivity with a concentration level between $1x10^{16} – 1x10^{19}$ atoms/cm^3.

14. The tri-gate device of claim 12 wherein said channel region of said semiconductor body is doped to a n type conductivity with a concentration level between $1x10^{16} – 1x10^{19}$ atoms/cm^3.

15. The tri-gate transistor of claim 9 wherein said thin film completely surrounds said semiconductor body and said gate electrode.

16. The method of claim 9 wherein a thin grown oxide layer is formed between the bottom of said semiconductor body and said thin film.

17. A method of forming a semiconductor device comprising:

forming a semiconductor body having a top surface and laterally opposite sidewalls on a insulating substrate;

forming a gate dielectric on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

forming a gate electrode on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

forming a thin film adjacent to said semiconductor body wherein said thin film produces a stress in said semiconductor body.

18. The method of claim 17 wherein said thin film produces a compressive stress in said semiconductor body.

19. The method of claim 17 wherein said thin film produces a tinsel stress in said semiconductor body.

20. The method of claim 17 wherein said thin film has a tinsel stress.

21. The method of claim 17 wherein said thin film has a compressive stress.

22. The method of claim 17 wherein said semiconductor body comprises a single crystalline silicon film.

23. The method of claim 17 wherein said semiconductor body is selected from the group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb, and carbon nanotubes.

24. A method of forming nonplanar transistor comprising:

patterning a monocrystalline silicon film formed on an insulating substrate into a silicon body having a top surface opposite a bottom surface formed on said insulating film, and a first and second laterally opposite sidewalls;

forming a gate dielectric layer on said top surface of said silicon body and on said sidewalls of said silicon body;

depositing a gate material over said silicon body and over said insulating substrate;

patterning said gate material to form a gate electrode on said gate dielectric layer on said top surface of said silicon body in adjacent to said gate dielectric on said sidewalls of said silicon body, said gate electrode having laterally opposite sidewalls which run perpendicular to said laterally opposite sidewalls of said silicon body;

forming a pair of source/drains regions in said silicon body on opposite sides of said laterally opposite sidewalls of said gate electrode, wherein the region between said source/drain regions in said silicon body forms a channel region;

removing a portion of said insulating substrate from underneath a portion of channel region of said silicon body and beneath a portion of said source and drain regions of said silicon body; and

forming a film having a stress therein beneath said exposed portion of said silicon body beneath said gate electrode and beneath said exposed portion of said source and drain regions beneath said gate electrode.

25. The method of claim 24 wherein said thin film has compressive stress which produces a tinsel stress in said channel region.

26. The method of claim 24 wherein said thin film has a tinsel stress which produces a compressive stress in said channel region of said semiconductor body.

27. The method of claim 24 further comprising forming said thin film adjacent to said laterally opposite sidewalls of said silicon body and said laterally opposite sidewalls of said gate electrode.

28. The method of claim 24 wherein said formation of said thin film is continued until said silicon body and said gate electrode are completely surrounded by said thin film.

29. The method of claim 24 further comprising oxidizing said bottom portion of said semiconductor body after exposing said semiconductor body and prior to forming said thin film.